

In the Claims:

1. (currently amended) A method of manufacturing a semiconductor device, comprising:
forming a gate oxide over a substrate and a gate electrode over the gate oxide;
implanting impurities into the substrate using the gate electrode as an implant mask to form lightly-doped regions in the substrate;
forming a first spacer adjacent the gate electrode;
implanting impurities into the substrate and through a portion of the lightly-doped regions using the first spacer as an implant mask to form deep source/drain regions in the substrate;
forming a second spacer adjacent the first ~~spacer~~; spacer, wherein the second spacer comprises a low thermal budget oxide formed with a thermal budget of less than 600 degrees

Celsius;

- implanting impurities into the substrate using the second spacer as an implant mask to form a graded source/drain region in the substrate; and
removing the second spacer.
2. (original) The method as recited in Claim 1, wherein said first spacer comprises a nitride.
3. (currently amended) The method as recited in ~~Claim 1~~ Claim 7, wherein said second spacer comprises an oxide.
4. (original) The method as recited in Claim 3, wherein the second spacer is a low-temperature oxide having a thermal budget of less than 600C.

5. (currently amended) ~~The method as recited in Claim 1, further including~~ A method of manufacturing a semiconductor device, comprising:

forming a gate oxide over a substrate and a gate electrode over the gate oxide;

implanting impurities into the substrate using the gate electrode as an implant mask to form lightly-doped regions in the substrate;

forming a first spacer adjacent the gate electrode;

implanting impurities into the substrate and through a portion of the lightly-doped regions using the first spacer as an implant mask to form deep source/drain regions in the substrate;

forming a second spacer adjacent the first spacer;

implanting impurities into the substrate using the second spacer as an implant mask to form a graded source/drain region in the substrate;

removing the second spacer; and

depositing a nitride layer over the gate electrode and lightly-doped regions and forming the first spacer from the nitride layer, and further including depositing an oxide layer over the gate electrode and lightly-doped regions and forming the first spacer from the oxide layer.

6. (original) The method as recited in Claim 1, further including forming a salicide over the source/drain regions.

7. (currently amended) ~~The method as recited in Claim 1, further including:~~ A method of manufacturing a semiconductor device, comprising:

forming a gate oxide over a substrate and a gate electrode over the gate oxide;

implanting impurities into the substrate using the gate electrode as an implant mask to form lightly-doped regions in the substrate;

forming a first spacer adjacent the gate electrode;
implanting impurities into the substrate and through a portion of the lightly-doped regions
using the first spacer as an implant mask to form deep source/drain regions in the substrate;
forming a second spacer adjacent the first spacer;
implanting impurities into the substrate using the second spacer as an implant mask to
form a graded source/drain region in the substrate;
removing the second spacer;
forming a dielectric over the gate electrode and the deep source/drain regions;
forming a contact opening through said dielectric; and
forming an interconnect in said contact opening, the interconnect being electrically
coupled to the deep source/drain regions.

8. (currently amended) A method of manufacturing a semiconductor device, comprising:
- forming a gate oxide over a substrate and a gate electrode over the gate oxide;
- implanting impurities into the substrate using the gate electrode as an implant mask to
form lightly-doped regions in the substrate;
- forming a first spacer adjacent the gate electrode;
- forming a second spacer adjacent the first spacer; spacer, wherein the second spacer
comprises a low thermal budget oxide formed with a thermal budget of less than 600 degrees
Celsius;
- implanting impurities into the substrate using the second spacer as an implant mask to
form a graded source/drain region in the substrate;
- removing the second spacer; and

implanting impurities into the substrate and through a portion of the lightly-doped regions using the first spacer as an implant mask to form deep source/drain regions in the substrate.

9. (original) The method as recited in Claim 8, wherein said first spacer comprises a nitride.

10. (currently amended) The method as recited in ~~Claim 8~~ Claim 12, wherein said second spacer comprises an oxide.

11. (original) The method as recited in Claim 10, wherein the second spacer is a low-temperature oxide having a thermal budget of less than 600C.

12. (currently amended) ~~The method as recited in Claim 8, further including~~ A method of manufacturing a semiconductor device, comprising:

forming a gate oxide over a substrate and a gate electrode over the gate oxide;

implanting impurities into the substrate using the gate electrode as an implant mask to form lightly-doped regions in the substrate;

forming a first spacer adjacent the gate electrode;

forming a second spacer adjacent the first spacer;

implanting impurities into the substrate using the second spacer as an implant mask to form a graded source/drain region in the substrate;

removing the second spacer;

implanting impurities into the substrate and through a portion of the lightly-doped regions using the first spacer as an implant mask to form deep source/drain regions in the substrate; and

depositing a nitride layer over the gate electrode and lightly-doped regions and forming the first spacer from the nitride layer, and further including depositing an oxide layer over the gate electrode and lightly-doped regions and forming the first spacer from the oxide layer.

13. (original) The method as recited in Claim 8, further including forming a salicide over the source/drain regions.

14. (currently amended) ~~The method as recited in Claim 8 further including:~~ A method of manufacturing a semiconductor device, comprising:

forming a gate oxide over a substrate and a gate electrode over the gate oxide;

implanting impurities into the substrate using the gate electrode as an implant mask to form lightly-doped regions in the substrate;

forming a first spacer adjacent the gate electrode;

forming a second spacer adjacent the first spacer;

implanting impurities into the substrate using the second spacer as an implant mask to form a graded source/drain region in the substrate;

removing the second spacer;

implanting impurities into the substrate and through a portion of the lightly-doped regions using the first spacer as an implant mask to form deep source/drain regions in the substrate;

forming a dielectric over the gate electrode and the source/drain regions;

forming a contact opening through said dielectric; and

forming an interconnect in said contact opening, the interconnect being electrically coupled to said source/drain regions.

Please cancel Claims 15-20.

21. (new) A method of manufacturing a semiconductor device, comprising:
- forming a gate oxide over a substrate and a gate electrode over the gate oxide;
 - implanting impurities into the substrate using the gate electrode as an implant mask to form HALO pocket regions;
 - implanting impurities into the substrate using the gate electrode as an implant mask to form lightly-doped regions in the substrate, wherein at least part of the HALO pocket regions extend below the lightly-doped regions;
 - forming a first spacer adjacent the gate electrode;
 - implanting impurities into the substrate and through a portion of the lightly-doped regions using the first spacer as an implant mask to form deep source/drain regions in the substrate;
 - forming a second spacer adjacent the first spacer;
 - implanting impurities into the substrate using the second spacer as an implant mask to form a graded source/drain region in the substrate; and
 - removing the second spacer.
22. (new) The method as recited in Claim 21, wherein the first spacer comprises a nitride.
23. (new) The method as recited in Claim 21, wherein the second spacer comprises an oxide.
24. (new) The method as recited in Claim 23, wherein the oxide of the second spacer is a low thermal budget oxide formed with a thermal budget of less than 600 degrees Celsius.

25. (new) The method as recited in Claim 21, further including depositing a nitride layer over the gate electrode and lightly-doped regions and forming the first spacer from the nitride layer, and further including depositing an oxide layer over the gate electrode and lightly-doped regions and forming the first spacer from the oxide layer.

26. (new) The method as recited in Claim 21, further including forming a salicide over the source/drain regions.

27. (new) The method as recited in Claim 21, further including:
forming a dielectric over the gate electrode and the deep source/drain regions;
forming a contact opening through the dielectric; and
forming an interconnect in the contact opening, the interconnect being electrically coupled to the deep source/drain regions.